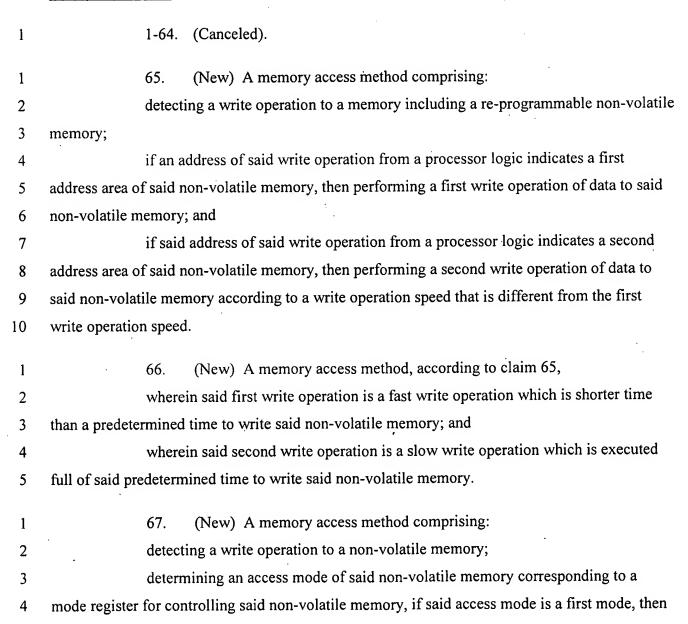
## Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application. In the listing below, inserted text is marked with <u>underline</u>, deleted text is marked with <u>strikethrough</u>, and changes are identified by a vertical bar in the margin.

## **Listing of Claims:**



5	performing a fast write operation of data to said non-volatile memory, if said access mode is a
6	second mode, then performing a slow write operation of data to said non-volatile memory,
7	if said access mode is a third mode write operation, then:
8	if an address of said non-volatile memory from a processing logic is
9	indicated a first address area, then said non-volatile memory is executed said fast write
10	operation of data,
11	if an address of said non-volatile memory is indicate a second address
12	area, then said non-volatile memory is executed said slow write operation of data; and
13	if said access mode is a fourth mode, then performing a cache write operation of
14	data to a cache memory comprised a random access memory based on an exception handler
15	routine.
1 .	68. (New) A memory access method, according to claim 67,
2	wherein if a cache line of said cache memory stores other data in said cache write
3	operation of said data, said other data is written to said non-volatile memory and said data is
4	written to said cache line of said cache memory.
7	written to said eache file of said eache memory.
1	69. (New) A memory access method, according to claim 67,
2	wherein said mode register is indicated access mode for said non-volatile
. 3	memory.
1	70 (May) A mamory access method, according to claim 68
l 2	70. (New) A memory access method, according to claim 68, wherein said slow write operation has a predetermined write time to said non-
2	
3	volatile memory; and  wherein said fast write operation has a write time shorter than said predetermined
4	time of said slow write time.
5	time of said slow write time.
1	71. (New) A memory access method, according to claim 67,
2	wherein said first address area and said second address area is indicated in a
3	register.

1	72. (New) A memory access method according to claim 65, wherein detecting
2	a write operation to the re-programmable non-volatile memory is based on identifying the write
3	operation as directed to a predetermined address space that corresponds to the re-programmable
4	non-volatile memory.
1	73. (New) A data processing unit comprising:
2	memory, including a re-programmable non-volatile memory; and
3	control logic configured for detecting a write operation to the memory and for
4	performing said write operation according to an operation mode in which the control logic
5	determines if an address of said write operation from a processor logic indicates a first address
6	area of said non-volatile memory and performs a first write operation of data to said non-volatile
7	memory, and if said address of said write operation from a processor logic indicates a second
8	address area of said non-volatile memory, then performs a second write operation of data to said
9	non-volatile memory.
1	74. A data processing unit according to claim 73, wherein the control logic
2	detects a write operation to the re-programmable non-volatile memory by identifying the write
3	operation as directed to a predetermined address space that corresponds to the re-programmable
4	non-volatile memory.